Application No.: 10/052,736 Docket No.: SON-2313

AMENDMENTS TO THE ABSTRACT

Please substitute the following paragraph(s) for the abstract now appearing in the currently filed specification:

period of a specific address test pattern in testing a semiconductor device. The semiconductor testing apparatus includes test pattern memory means adapted for storing and managing test pattern data in accordance with addresses, and outputting the test pattern specified by the desired address; test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from the memory means; and control means for controlling the test pattern memory means and the test pattern generation means in such a manner that the test pattern signal based on the test pattern data of the desired address can be generated at a predetermined timing conforming with the set information. --